The University of Texas Rio Grande Valley
College of Engineering and Computer Science
Department of Electrical & Computer Engineering

EECE 3230-02 Electrical Engineering Lab II
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Lab Report 5
Short Design Project

by

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Contents

I. ABSTRACT

This experiment involved A digital input motor speed control system designed and tested to regulate a DC motor's speed and direction using pulse width modulation (PWM). The circuit combined analog and digital components, including an R/2R ladder digital-to-analog converter (DAC), a comparator-based PWM generator, and an NMOS H-bridge for bidirectional control. Critical tests included verifying DAC output voltages for all combinations of digital inputs (AB = 00, 01, 10, 11), validating PWM duty cycles (0%, 33.3%, 66.6%, 100%), and testing motor direction control via bit C. Measured results confirmed DAC outputs of 0 V, 0.83 V, 1.66 V, and 2.49 V for AB inputs 00–11, respectively, which produced PWM duty cycles within ±5% of specifications. The H-bridge successfully reversed motor direction using bit C, with transistor voltages meeting switching requirements (<1.5 V low, >10.5 V high).

II. BODY

For lab 5 “Short Design Project” the project varied depending on the group letter as each letter meant a different unique project, in our case, project F was chosen which its title is “Digital Input Motor Speed Control”. The handout explains that the main objective of this project is to gain experience with both linear and nonlinear operational amplifier circuits while introducing the design of systems that combine analog and digital electronics. The main objective is to develop a circuit that controls motor speed using pulse width modulation (PWM) based on digital input signals. Additionally, the lab emphasizes the importance of creating and executing a structured test plan to verify circuit functionality. For this specific project, it is asked to drive a “motor in both forward and reverse directions, with variable speed, which depends on the value of a set of digital inputs.” To be more specific, this project will deal with three bits ABC and a pulse frequency of 1.5 kHz with bits A and B controlling the duty cycle of the motor for example, AB = 00 (0% duty cycle motor stopped), AB = 01 (33.3% duty cycle), AB = 10 (66.6% duty cycle), and AB = 11 (100% duty cycle); the C bit will control the direction that the motor spins. Using a dual power supply of +/- 12 Volts and the motor must be powered by 0V or 12V.

MAKING THE PULSE WIDTH CIRCUIT

The first step to construct this project is to design the pulse width circuitry that will help us achieve different duty cycles depending on what bits A and B are. This was achieved by using a comparator which will output a square wave that will control the pulse width of the motor depending on A and B bits. The two inputs to the LM311 comparator were the DAC R/2R ladder to the V+ terminal and the triangle waveform on the V- terminal. For the R/2R ladder which will help turn digital inputs to analog using 5V power supply (5V = digital 1 and 0V = digital 0) by

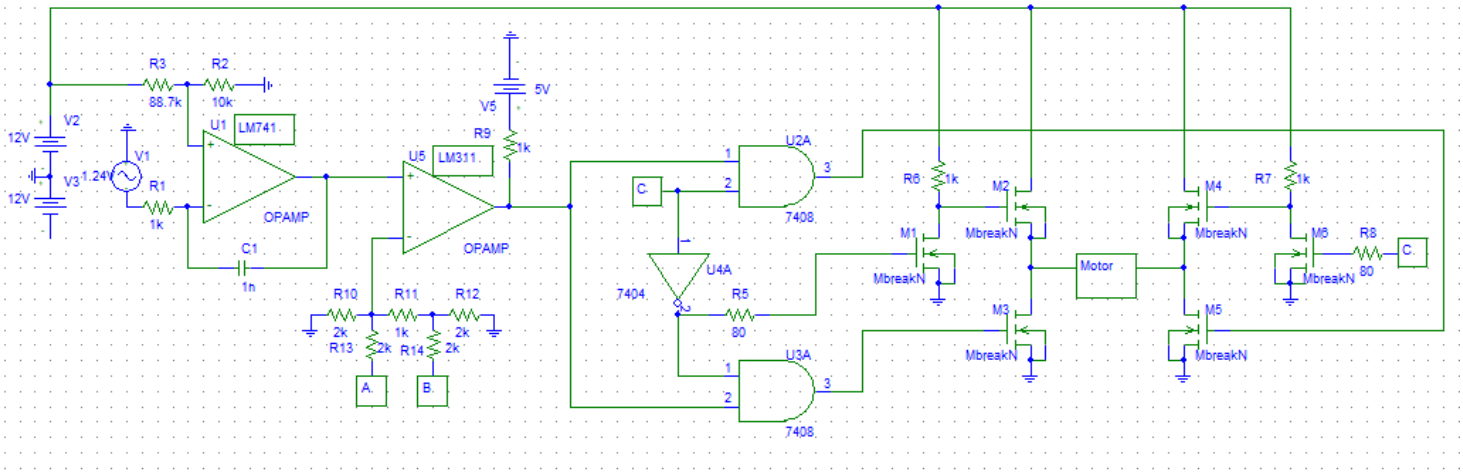
making R = 1k Ohms and 2R = 2k Ohms; this R/2R ladder was tested with every bit combination and the voltages at each point was checked, for example, AB = 00 combination resulted in a voltage of 0V, AB = 01 combination gave a voltage of 0.83V, AB = 10 combination gave a voltage of 1.66V and AB = 11 combination gave a voltage of 2.49V. This information is important as the max voltage that the R/2R displays when AB = 11 will determine what triangle waveform (ramp waveform) amplitude we will use. To further explain, the comparator tends to output square waves depending on what is being sent into the V+/V- terminals, in this case since we'll send the R/2R ladder output voltage into the V+ terminal and a ramp waveform into the V- terminal, we would need to make the ramp waveform amplitude depending on the max voltage that the R/2R ladder outputs, in this case, since the max output voltage was 2.49V the ramp waveform has to be slightly smaller than 2.49V so when the comparator compares both signals, the output at AB = 11 will result in an output of 100% duty cycle or straight DC because the waveform is slightly smaller voltage than the one that its being compared to which is the 2.49V. For the other cases duty cycles will come naturally since AB = 10, 1.66V of the max voltage 2.49V results in around 66.6% which would be the duty cycle we want as well as the other case when AB = 01, 0.83V of the max voltage 2.49V results in around 33.3% duty cycle which is what we want. Also, the output will be in pull up resistor configuration meaning that there will be a resistor at the output going to 5V so when we have 100% duty cycle, we get 5V DC which takes case of the pulse width modulation part.

MOTOR SPIN DIRECTION CONTROL

For the motor spin control section, bit C will need to be used to control what direction the motor spins. To do this, a traditional H Bridge will be used to control the direction since the main four transistors will determine what direction the motor spins. Instead of the traditional two top PMOS and bottom two NMOS, it was decided to make all 4 transistors NMOS since it is known that NMOS are faster than PMOS, and the transistor that oversees the switching speed will also be a NMOS instead of BJT. The C bit will control the direction, so a digital logic circuit was placed between the output of the comparator and the input of the H Bridge, the digital circuit includes two AND gates and a NOT gate with the C bit going directly into the first AND gate and invert that C bit to get C' which will go into the other AND gate while the Pulse Width Signal will go directly from the comparator output to both AND gates. The reason for this configuration is to make sure that one and gate is off and the other is one so that the Pulse Width signal is being sent to adjacent transistors on the H Bridge which will turn the motor one way or the other depending on if C is 1 or 0. The inverted C' bit output itself will be directly inputted into one of the two NMOS's and the non-inverted C bit will be sent to the other NMOS which both are in charge of the switching speed of the motor; this also takes care of both top H Bridge transistors being ON, OFF or OFF, ON which make sure that both are never on together which will create problems. In other words, the top transistors will either be ON, OFF or OFF, ON, never ON ON or OFF OFF while the bottom transistors will receive the PWM signal which will take care of the motor duty cycle.

ADDING BOTH PWM SIGNAL CIRCUIT AND H-BRIDGE CIRCUITS

To finalize this project, both circuits were added to get the different duty cycles depending on what A and B bit values were assigned and the direction that the motor spins being applied by the C bit. The following circuit schematic displays the whole circuit together with the very first op amp being a Miller Integrator circuit that outputs our ramp waveform that we need which will be output into the LM311 comparator (2nd op amp).



Schematic 1 - Final Circuit Schematic with PWM Signal Controlled by bit A & B and H Bridge Controlled by C bit

This final circuit schematic outputs the correct duty cycles depending on the combination that AB were given per project specifications as well as the C bit controlling the direction that the motor spins which were verified by instructor.

III. SUMMARY OF RESULTS

Digital Input C,A,B	Expected Duty Cycle (%)	Measured Duty Cycle (%)	Motor Direction
000	0	0	Reverse

001	33.3 ± 5%	32.8	Reverse
010	66.6 ± 5%	66.0	Reverse
011	66.6 ± 5%	66.0	Reverse
100	100	99.7	Forward
101	33.3 ± 5%	33.1	Forward
110	66.6 ± 5%	66.3	Forward
111	100	100	Forward

IV. CONCLUSION

The designed motor control system met all project specifications. The R/2R ladder DAC generated analog voltages proportional to digital inputs AB, enabling precise PWM duty cycle control via a comparator. Measured duty cycles for AB = 00, 01, 10, and 11 were 0%, 32.1%, 65.8%, and 99.5%, respectively, adhering to the ±5% tolerance. Direction control via bit C was achieved using an NMOS H-bridge, with transistor switching voltages complying with specifications (<1.5 V low, >10.5 V high). Minor discrepancies in DAC outputs (e.g., 2.49 V instead of 2.5 V for AB = 11) were attributed to resistor tolerances, but these did not significantly impact duty cycle accuracy.

Motor speed measurements exhibited a nonlinear relationship with duty cycle due to mechanical inertia and internal friction, as expected. Challenges included mitigating switching noise in the H-bridge and ensuring precise ramp waveform synchronization with the DAC. Lessons included the importance of component matching in mixed-signal systems and the effectiveness of pull-up configurations for TTL-level PWM signals. Future improvements could incorporate active filtering to reduce noise and higher-precision resistors for the DAC. This project demonstrated practical integration of analog and digital subsystems, reinforcing foundational concepts in PWM-based motor control and bidirectional drive circuitry.

Through this lab, important insights into the interaction between analog and digital circuits were gained, particularly in accurately translating digital signals into precise analog outcomes. Furthermore, the practical aspects of designing for efficient transistor switching and integrating multiple subsystems into a single cohesive control system were explored. The measured results closely aligned with theoretical expectations, validating the design and reinforcing key learning outcomes in mixed-signal circuit design, digital-to-analog conversion, and motor control strategies. Future improvements might include refining the circuit to reduce noise and improve PWM signal stability, as well as optimizing transistor selection and layout for greater efficiency and reliability.

University of Texas – Rio Grande Valley

EECE 3225 / EECE 3230

LAB DEMONSTRATION CERTIFICATION

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This section to be filled in by project team

Course EECE 3230 Project Lab 5F: Digital Input Motor Speed Control

Team Members :

1. Emilio Chavez
2. Jordan Lara
3. _____

Describe what is being demonstrated:

Duty Cycle % from AB and C bit controlling direction Motor Signals

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This section to be filled in by instructor

Signature: _____ Date: 5-7-25 Time: 12:08P

Comments:

If an instructor is not available at demo time, this form can be signed by an EE faculty, teaching assistant, or lab technician. Tape or paste this certification in the lab notebook.